AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A memory module including a non-volatile memory, a dynamic random access memory, a static random access memory, and a control circuit that accesses the non-volatile memory, the dynamic random access memory, and the static random access memory, the memory module comprising:

a dynamic random access memory interface to outside the memory module for accessing the dynamic random access memory from outside the memory module; and

a static random access memory interface to outside the memory module for accessing the static random access memory from outside the memory module,

wherein the dynamic random access memory interface is arranged to connect to a first memory controller outside the memory module, ~~and~~

wherein the static random access memory interface is arranged to connect to a second memory controller outside the memory module, different from the first memory controller, and

wherein, when data stored in the non-volatile memory is to be outputted to outside the memory module, data stored in the non-volatile memory is transferred to at least one of the dynamic random access memory and the static random access memory, and then any portion of said data transferred to the dynamic random access memory is outputted to outside the memory module via the dynamic random access memory interface, and any portion of said data transferred to the static random access memory is outputted to outside the memory module via the static random access memory interface.

2. (original) A memory module according to Claim 1, wherein:

immediately after power is turned on, data in a predetermined address region of the non-volatile memory is transferred to the static random access memory.

3. (original) A memory module according to Claim 1, wherein:

immediately after power is turned on, data in a predetermined address region of the non-volatile memory is transferred to the dynamic random access memory.

4. (previously presented) A memory module according to Claim 1, wherein:

data transfer between the non-volatile memory and the dynamic random access memory is performed according to an instruction sent via the dynamic random access memory interface.

5. (previously presented) A memory module according to Claim 1, wherein:

data transfer between the non-volatile memory and the static random access memory is performed according to an instruction sent via the static random access memory interface.

6. (previously presented) A memory module according to Claim 1, wherein:

in transferring data from the non-volatile memory to the static random access memory or the dynamic random access memory, data having an error is corrected before being transferred.

7. (previously presented) A memory module according to Claim 1, wherein:

in transferring data from the static random access memory or the dynamic random access memory to the non-volatile memory, an address replacement process is executed.

8. (original) A memory module according to Claim 1, wherein:

a boot program is held in the non-volatile memory.

9. (previously presented) A memory module according to Claim 1, wherein:

data transfer range data, which includes a range of data transferred from the non-volatile memory to the dynamic random access memory at initial time when operating power is turned on, is held in the non-volatile memory.

10. (previously presented) A memory module according to Claim 1, wherein:

the static random access memory has a memory size equal to or smaller than 1/1000 of the memory size of the non-volatile memory.

Claim 11. (cancelled)

12. (previously presented) A memory module according to Claim 1, wherein:

a data-hold operation of the dynamic random access memory is executed inside the memory module.

Claim 13. (cancelled)

14. (previously presented) A memory module according to Claim 12, wherein:

the memory module is accessed first;

the dynamic random access memory performs a data-hold operation second; and

the memory module performs data transfer between the non-volatile memory and the static random access memory or the dynamic random access memory third.

15. (previously presented) A memory module according to Claim 1, wherein:

the dynamic random access memory is synchronous DRAM; and

access to the non-volatile memory and the dynamic random access memory from outside the memory module is made via the dynamic random memory access interface.

16.   (original) A memory module according to Claim 1, wherein:

the non-volatile memory is a NAND flash memory; and

the dynamic random access memory is synchronous DRAM.

17.   (original) A memory module according to Claim 1, wherein:

the non-volatile memory is an AND flash memory; and

the dynamic random access memory is synchronous DRAM.

Claims 18-20. (cancelled)

21.   (previously presented) A memory module according to Claim 1, wherein:

the dynamic random access memory includes plural interfaces.

Claims 22-23. (cancelled)

24.   (previously presented) A memory module according to Claim 1, wherein:

the dynamic random access memory includes a control circuit which processes access from the outside of the

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memory module and a control circuit that independently

accesses the non-volatile memory.

25. (previously presented) A memory module according

to Claim 1, wherein:

the dynamic random access memory includes a control

circuit to independently access the non-volatile memory and

a circuit to subordinately process the access.

Claim 26. (cancelled)

27. (previously presented) A memory module according

to Claim 1, wherein:

the non-volatile memory includes a static random access

memory, an error detecting and correcting circuit, and an

address replacement circuit.

28. (previously presented) A memory module according

to Claim 1, wherein:

the non-volatile memory includes plural interfaces.

Claims 29-78. (cancelled)

79. (previously presented) A memory module according to Claim 1, wherein:

said accessing the dynamic random access memory is from a device outside the memory module.